**ECE 429 Lab 3**

**Inverter Layout**

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**Introduction**

The objective of this lab is to use VLSI design to design and test an inverter layout. The secondary objective is to gain experience creating layouts within an industrial setting.

**Theory/Pre-Lab**

A layout editor is used to design layouts in a platform not unlike a painting program. It is important that layouts follow a methodology to design as described in the lab manual. For different designs and technologies, there are also Layout Design Rules. It is common practice for layout designs to perform design rule checking throughout the layout process. A Layout vs. Schematic (LVS) tool is used to ensure that the Layout matches with the intended schematic.

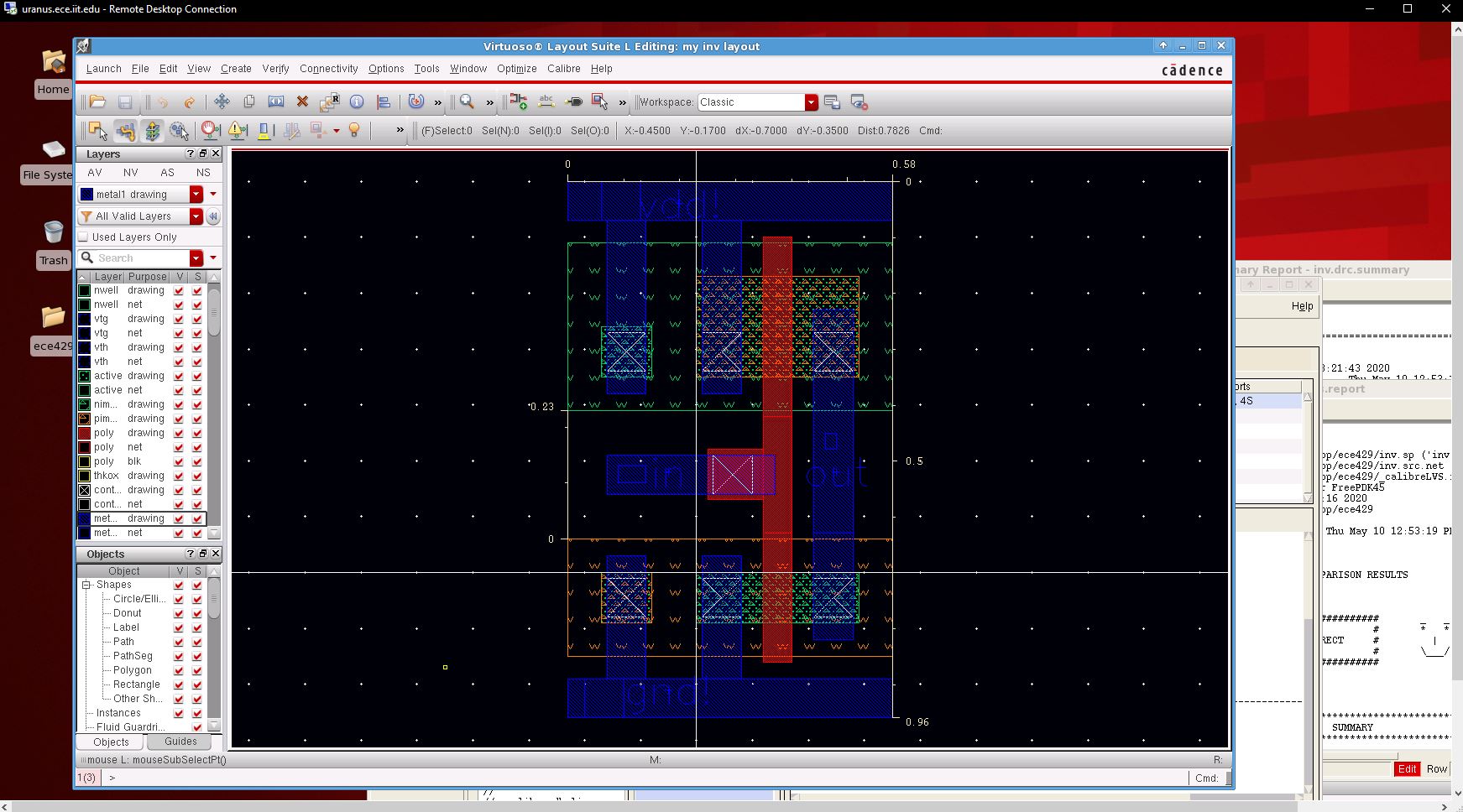
Calibre will be used as both the Design Rule Checking (DRC) tool and the LVS tool. It is integrated into the Virtuoso platform. Calibre PEX will be used to extract parasitic capacitances from the layout that is created. HSPICE will then be used to simulate the circuit.

Prior to the lab, the FREEPDK45 design rules were read and studied. The Tutorial II: Inverter Layout was also read.

**Implementation**

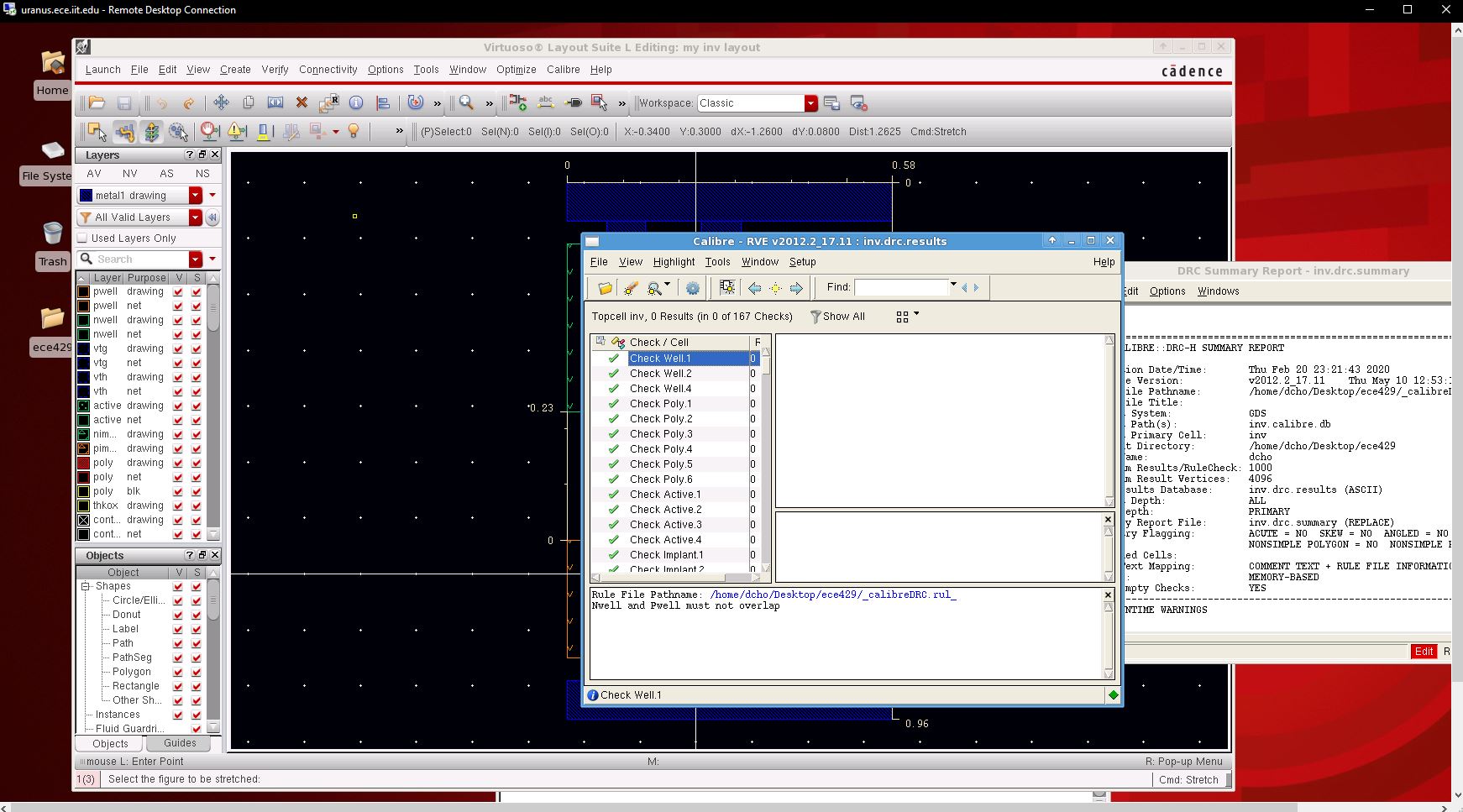
By following the tutorial and using Virtuoso, the following layout was created.

**Figure 1: Inverter Layout**



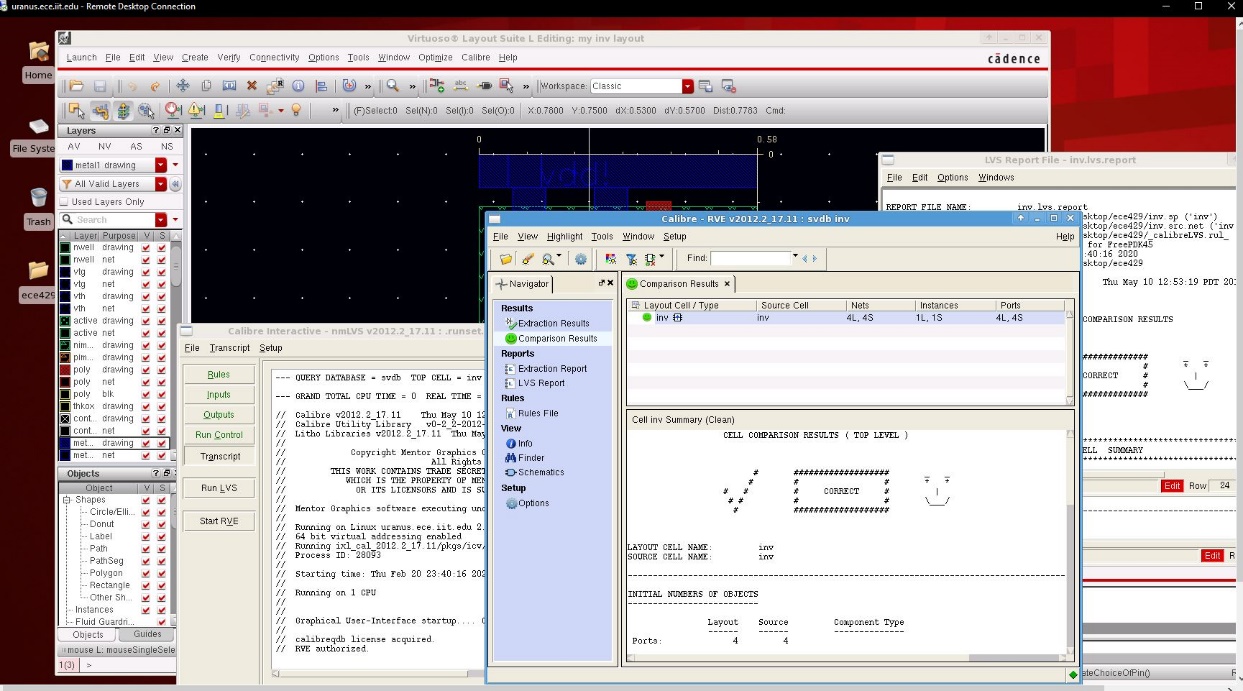
The layout follows logic of the inverter schematic from Lab 2. While creating the layout, a DRC was frequently run to check if the layout was following the rules.

**Figure 2: DRC**

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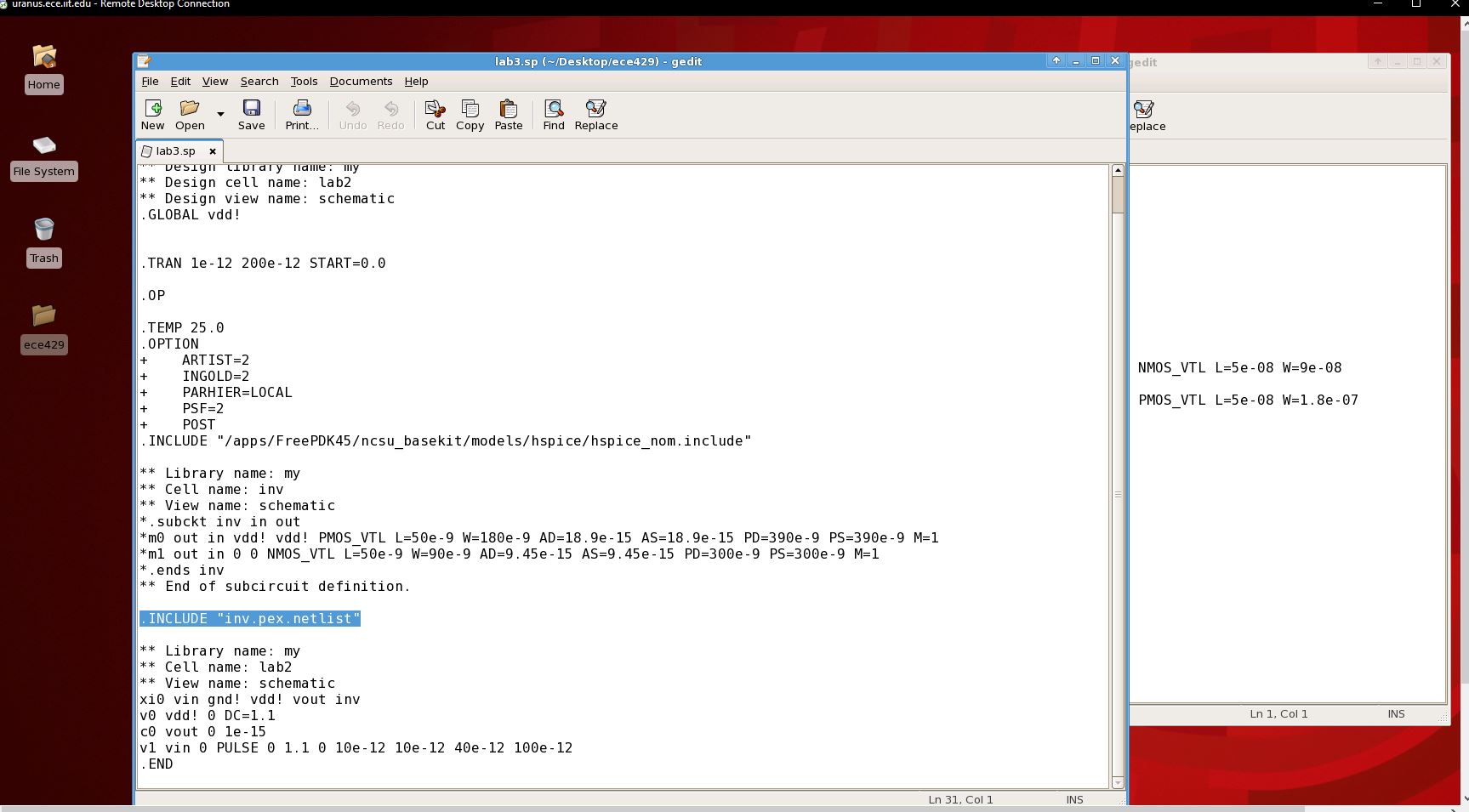
Once the DRC was passed, the next part was to make sure that the layout matched the inverter schematic. This was done using LVS. The pass can be seen below.

**Figure 3: LVS**

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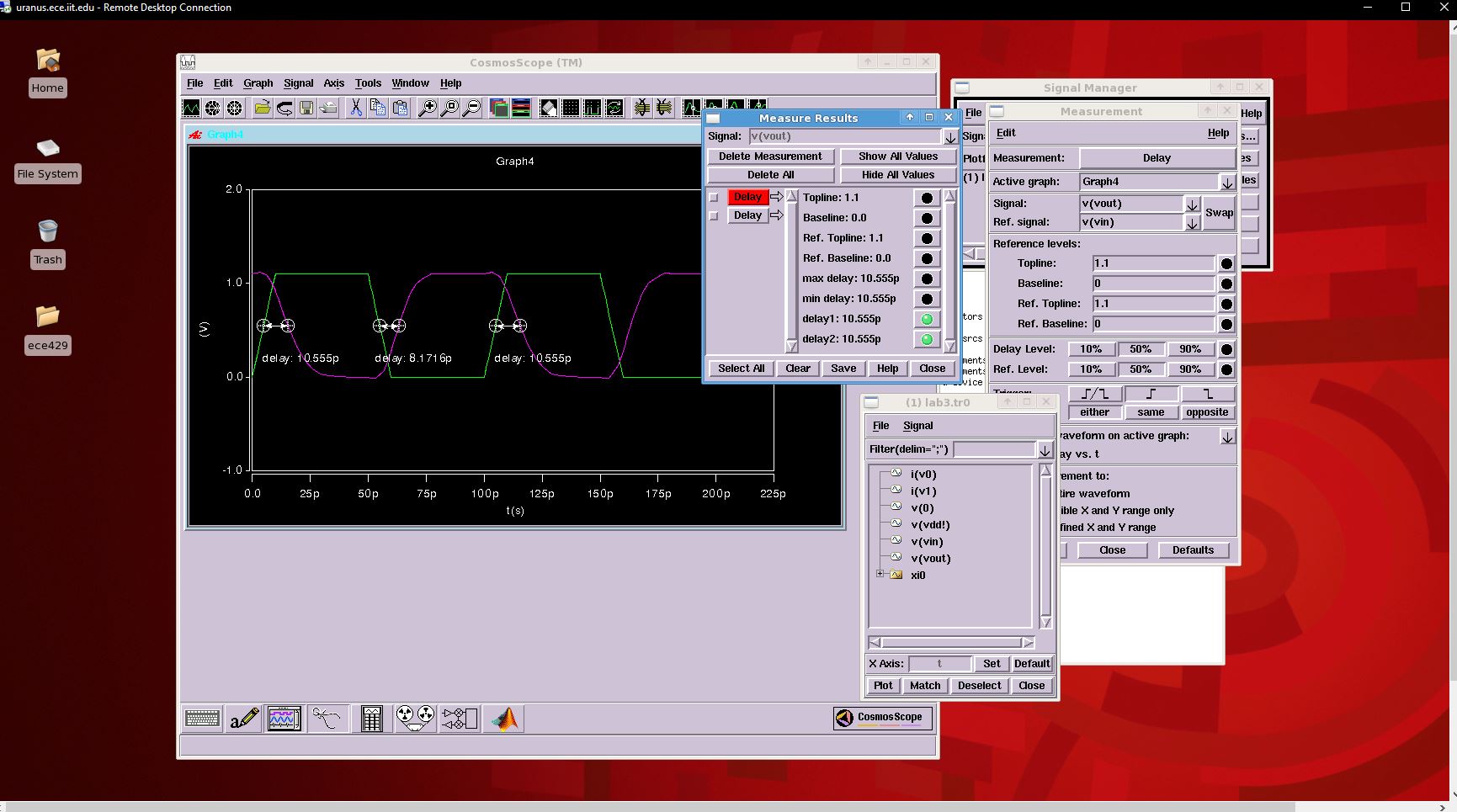
As can be seen above, the layout matches the inverter schematic from Lab 2. In order to test the layout, HSPICE was used. The .sp file needed to be edited to read from the layout .pex file.

**Figure 4: Modified Netlist**

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Once the netlist was edited, HSPICE was used. The results from the simulation was checked using CosmosScope

**Figure 5: HSPICE Simulation Result**

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The results were expected, as they are similar to the results from the tutorial manual.

**Deliverable Questions**

1. The minimum transistor width and length are determined by the necessary transistor performance for the specific technology. Smaller lengths allow the voltage gate to have a stronger influence in enabling current flow. Wider transistors have more channels for current to flow through.
2. Well-taps need to connect to implanted regions to avoid forward biasing the p-n junction.
3. Twin-well process allows the well regions to be independently optimized. PMOS and NMOS are well balanced in a twin-well process.
4. The delays are greater than those of Lab 2. This is expected because a schematic ignores the capacitance between layers (like the diffusion region) and other parasitic capacitances.

**Conclusion**

In conclusion, this lab was a success. The results were as expected and there were no particular difficulties. This lab made me more familiar with the Virtuoso platform, and did a good job introducing me to the Calibre program.